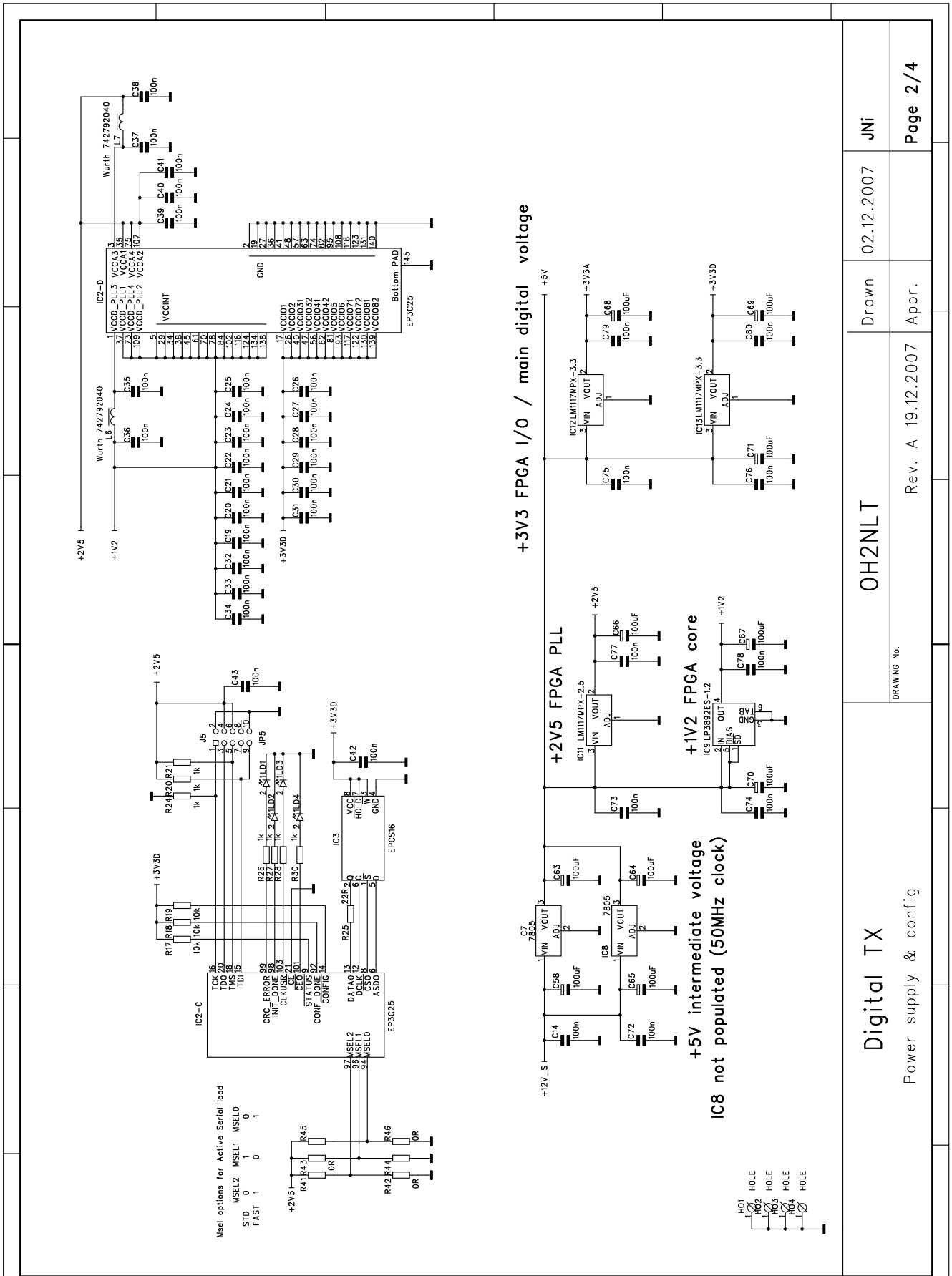
+3V3 FPGA I/O / main digital voltage
+2V5 FPGA PLL
+1V2 FPGA core
+5V intermediate voltage
IC8 not populated (50MHz clock)
Msel options for Active Serial load
MSEL2 MSEL1 MSEL0
STD 0 1 0
FAST 1 0 1
OH2NLT
Digital TX
Power supply & config
Drawn
02.12.2007
JNi
Appr.
Rev. A 19.12.2007
DRAWING No.
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